Tevatron Beam Loss Monitor Upgrade

Integrator/Digitizer Card Development

Every 20 us each of the four integrator values are digitized into a 16 bit words.

Samples from each channel are stored in a circular buffer in SRAM memory (16x64K per channel). Appropriate input and output pointers into the buffers are maintained.

The FPGA for the project is the Altera Cyclone part# EP1C6Q240C8.

For each of the four channels, three sums of different length are maintained. The length of each type of sum is writable from a processor on another card. There are only three types (not four times three).

The sums are maintained in registers within the FPGA

The sums are computed in the following manner:

1. The latest sample is added to each of the three sums for the channel.
2. The oldest sample that was part of the sum is subtracted off.
3. Note that the oldest sample is different for each of the three sums

Circular buffer pointers that point to the oldest sample in each sum must be maintained. These “Tail” pointers will not increment until the number of samples in a sum has reached its specified length.

Each 20 us the value of the Sums are compared to a threshold.

The threshold values are readable and writable from a processor on another card.

Each channel has a unique threshold for each of the three sums. Twelve thresholds in all.

The interface to the Tev Abort Control Bus is through the J2 connector. The pins have the following assignment

BLM Control Bus Backplane Signals

The abbreviations in the signal description are taken from the VMEbus Specification.
DVBM => Driven valid by the bus master.
DVBS => Driven valid by the selected slave.
DLBM => Driven low by the bus master, for active low signals.
DVBB => Driven valid by both slave and master.

Pin	Name	Description
A(13..1)	A[12..0]	Data transfer address lines (DVBM).
A15	MEMRD*	Active low during memory reads (DLBM).
A16	MEMWR*	Active low during memory writes (DLBM).
A17	WE*	Write Strobe (DLBM). Latch data on rising edge.
A(26..19)	D[7..0]	Data transfer data lines (DVBB).
A(31..28)	IRQ[3..0]	Interupt request lines (DVBM). NOT USED ON DIGITIZER CARD.
C2	spare1	Undefined signal received by Digitizer Card FPGA (DVBM).
C3	spare2	Undefined signal received by Digitizer Card FPGA (DVBM).
C5	ABORT0 (Immed.)	Immediate Abort status for selected channel (DVBS)
C6	ABORT1 (Fast)	Fast Abort status for selected channel (DVBS)
C7	ABORT2 (Slow)	Slow Abort status for selected channel (DVBS)
C8	ABORT3 (Very Slow)	Very Slow Abort status for selected channel (DVBS)
C9	AbortCS4	Board select bit (DVBM). Most significant bit.
C13	AbortCS3	Board select bit (DVBM).
C12	AbortCS2	Board select bit (DVBM). Least significant bit.
C11	AbortCS1	Channel select bit (DVBM). Most significant bit.
C10	AbortCS0	Channel select bit (DVBM). Least significant bit.
C15	Fast_LATCH(0)	Fast Sum Latch (DVBM). Latches current Fast Sum, for selected board/channel, for subsequent Read by Master.
C16	Slow_LATCH(1)	Slow Sum Latch (DVBM). Latches current Slow Sum, for selected board/channel, for subsequent Read by Master.
C17	VSlow_LATCH(2)	Very Slow Sum Latch (DVBM). Latches current Very Slow Sum, for selected board/channel, for subsequent Read by Master.
C19	AIP	Abort In Progress indication (DVBM). Digitizers will halt their data acquisition during this state.
C20	RESET_DC	Resets all sums (DVBM).
C21	RESET	*Currently undefined logic reset (DVBM).*
C22	MAKEMEAS	Data Acquisition Clock OR Data Acquisition Start Signal (DVBM).
C23	CYCLE_END	Signal to end data acquisition (DVBM).
C25	BusReq	NOT USED ON DIGITIZER CARD.
C26	BusAck	NOT USED ON DIGITIZER CARD.
C28	spare3	Undefined signal received by Digitizer Card FPGA (DVBM).
C29	spare4	Undefined signal received by Digitizer Card FPGA (DVBM).
C31	OSC	Control Bus Logic Oscillator (DVBM)